A 10mW, 4GHz CMOS Phase-Locked Loop with Dual-Mode Tuning Technique and Partly-Integrated Loop Filter

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***Abstract*—This publication presents the design of a 4GHz Integer-N frequency synthesizer with dual-mode tuning technique. The 3rd order loop filter is partly integrated. The intended application is a direct conversion UMTS transmitter. The design has been realized using a 0.12µm standard CMOS-process. The proposed advanced dual-mode tuning technique is based on digital coarse-tuning with subsequent analog fine-tuning. Therefore, the voltage controlled oscillator (VCO) features both, a digital and an analog tuning interface. This results in eight equidistant frequency bands. During coarse-tuning a digital control unit selects the correct frequency band for a certain frequency channel. The remaining frequency deviation is canceled through fine tuning, which is done by a conventional charge pump phase-locked loop (PLL) [5]. This results in lower spurious emission due to the smaller VCO gain. Lock-in times of 125µs were achieved. The output frequency can be tuned from 3.8GHz to 4.05GHz with a channel spacing of 400kHz. Except for the VCO with a supply voltage of 2.2V and a current consumption of 1.9mA to achieve higher output swing, the synthesizer is biased at 1.5V consuming 4mA. Thus, the overall power consumption can be stated with 10.2mW.**

I. INTRODUCTION

Frequency synthesis is among the major functions of RF radios. Transceivers require a frequency synthesizer to allocate different channels in a certain frequency band. In the past, most wireless systems have been implemented, using discrete components. For reasons like costs, size and power consumption, these designs are not optimal. Especially, the integration of high-quality (Q) passive components, like coils to achieve high phasenoise performance of oscillators with acceptable power consumption was the killing point of a single-chip solution for synthesizers [1-3]. To reduce resistance, today's CMOS technologies use copper as metallization. Tremendous CMOS scaling yields furthermore to a higher levels of integration, therefore reducing costs and power dissipation. This makes RF-CMOS solutions even more attractive for applications like PLLs [4,5].

This paper focuses on integer-N frequency synthesis with its building blocks for a UMTS transmitter [6]. The synthesizer is realized using a fully-integrated VCO. The proposed dual-mode tuning technique with its advantages is discussed in detail. Measurements of the achieved performance are presented. The designed was fabricated using a 0.12µm standard CMOS process.

II. DUAL-MODE TUNING CONCEPT

Figure 1 shows the major building blocks of the proposed Integer-N frequency synthesizer. The comparison frequency at the input of the phase-frequency detector (PFD) is 400kHz.

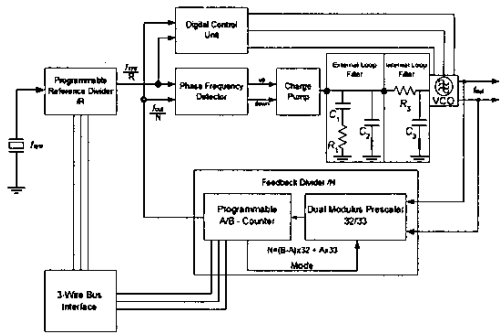

Figure 1. Integer-N frequency synthesizer with dual-mode tuning technique.

The two signals arise from the VCO (f_{out}) and the external reference clock (f_{sys}). A programmable reference divider ensures a flexible choice of f_{sys}, whereas the channel selection is done via the programmable feedback divider. The integer division ratios N are obtained with a high speed dual

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modulus prescaler in combination with a programmable modulus controller [7]. The programming is done via a 3-Wire bus interface. The PFD controls a cascoded charge pump. A 3rd order partly-integrated loop filter transforms the pulsed charge pump currents into an analog tuning voltage, controlling the frequency of the VCO. To perform coarse-tuning, an additional digital control unit is implemented in parallel to the phase-frequency detector. Depending on the selected output frequency, a three-bit digital word is generated to select the corresponding VCO band.

Figure 2(a) depicts a detailed block diagram of the proposed coarse tuning technique. The appropriate timing diagram is shown in figure 2(b).

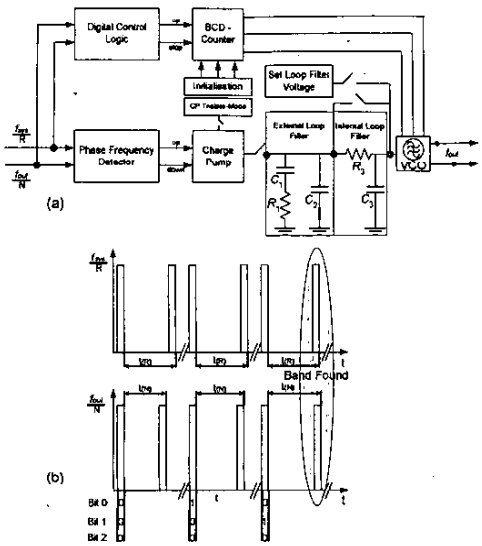

Figure 2. (a) Block diagram for digital coarse tuning. (b) Timing diagram.

Each time a new frequency channel is allocated by programming the feedback divider, the coarse-tuning sequence starts. At the same time the charge pump is switched to tristate mode, which is conterminous in disconnecting the loop filter from the charge pump. During coarse-tuning the loop filter is set to a fixed voltage. To achieve faster charging, the resistance R_3 is bypassed. The BCD-counter is initialized with a binary zero. This is equal to selecting the highest frequency band of the VCO (see figure 3). For proper coarse-tuning, both dividers must start at the same time, therefore they receive a synchronization signal. The period $t_{(VCO,N)}$ of the divided feedback signal is a function of the currently selected VCO band and the programmed divider ration N, whereas the divided reference signal has a constant period t_{ref}.

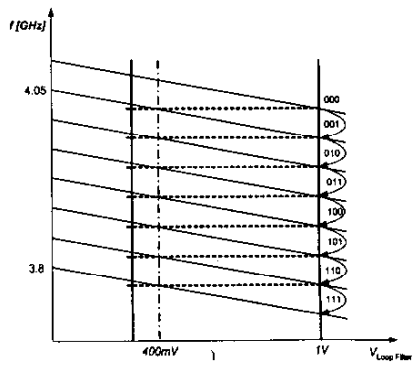

Figure 3. Simplified VCO tuning characteristic.

The digital control unit makes use of this fact and compares the timing of the incoming signals. If the feedback signal occurs before the reference signal the BCD-counter is incremented. This is equal to selecting the next lower frequency band of the VCO. The dividers are synchronized again. The correct frequency band is found when the above condition is not met anymore and the reference signal occurs before the feedback signal. From now on, the loop is closed again by connecting the charge pump to the loop filter. The applied constant voltage is disconnected and the resistor R_3 is part of the loop filter again. The remaining frequency deviation is now canceled by the charge pump controlled by the PFD. Each coarse-tuning step requires 2.5μs, this results in a total time of 20μs if all frequency bands are needed to allocate the desired output frequency f_{out}. To guarantee correct coarse-tuning, it is essential to note that there is sufficient overlap between adjacent VCO bands.

The major benefit of the dual-mode tuning technique is the minimization of the VCO gain, which results in lower spurious emission and better phasenoise performance. Another advantage is the limitation of the tuning voltage at the loop filter. The maximum tuning voltage is given by the constant voltage applied during coarse tuning, whereas the minimum voltage is determined by the frequency overlap of the adjacent VCO bands.

III. Technical Realization of the VCO

For the fully-integrated VCO, a complementary, differential architecture has been chosen, as depicted in figure 4(a) [8]. Cross-coupled NMOS- and PMOS-transistors (*M1-M4*) generate a negative re-

sistance to cancel the losses of the frequency determining LC-tank. The integrated inductance is realized as a fully-symmetrical octo-coil. To further reduce the series resistance of the inductor, the top three metal layers are connected in parallel. For the intended frequency range from 3.8GHz to 4.05GHz, the inductor achieves a measured quality factor of approximately 14.

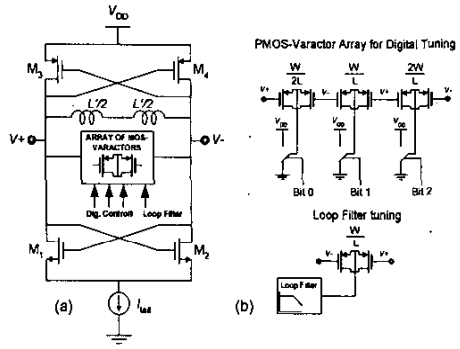

Figure 4. (a) Schematic of the LC-VCO (b) Varactor-array to support coarse tuning.

To support dual-mode tuning, the varactor consists of an array of binary-weighted PMOS-varactor blocks [9]. Three digital tuning inputs are controlled by the additional coarse tuning logic, while the analog tuning block is controlled by the loop filter voltage. Figure 5 shows the measured tuning characteristic of the free-running VCO.

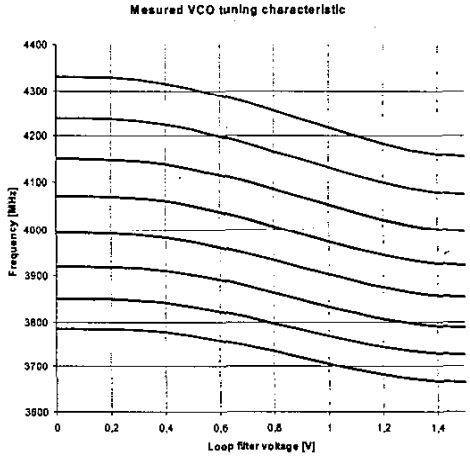

Figure 5. Tuning characteristic of the free-running VCO.

With a minimum oscillation frequency of 3.67GHz and a maximum oscillation frequency of 4.33GHz the VCO fulfills the specified tuning range with sufficient margin in case of process and temperature variations. For a proper operating charge pump at 1.5V supply the limitation of the loop filter voltage is given by 400mV and 1V. Within this span, the tuning characteristic shows a rather linear behavior with a VCO gain of 120MHz/V. To fulfill a tuning range of 660MHz within a span of 600mV, using a single varactor would result in a VCO gain of approximately 1.1GHz/V, which would drastically influence the performance of the PLL. Figure 6 shows the

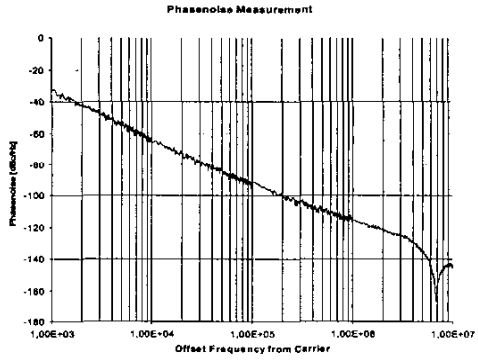

Figure 6. Phasenoise measurement of the free-running VCO.

achieved phasenoise performance of the free-running VCO.

IV. PLL Implementation and Experimental Results

The PLL with dual-mode tuning technique and partly-integrated loop filter was realized using a 0.12µm standard CMOS-process. Therefore, a four layer PCB has been constructed for all external connections like loop filter, supply und biasing network. The intended loop bandwidth for the UMTS transmitter application is 30kHz. The loop filter values were calculated in consideration of the PFD comparison frequency of 400 kHz, the VCO operating frequency with a gain of 120MHz/V, and the maximum charge pump current of 1.6mA.

TABLE I
SUMMARY OF LOOPFILTER VALUES

C_1	15nF (ext)
R_1	8.2kΩ (ext)
C_2	470pF (ext)
C_3	50pF (int)
R_3	20kΩ (int)

The summarized loop filter values in table I are with respect to figure 1. All measurements were performed using a Rhode & Schwarz FSP spectrum analyzer.

Figure 7 shows the measured output power spectral density at a carrier frequency of 4GHz.

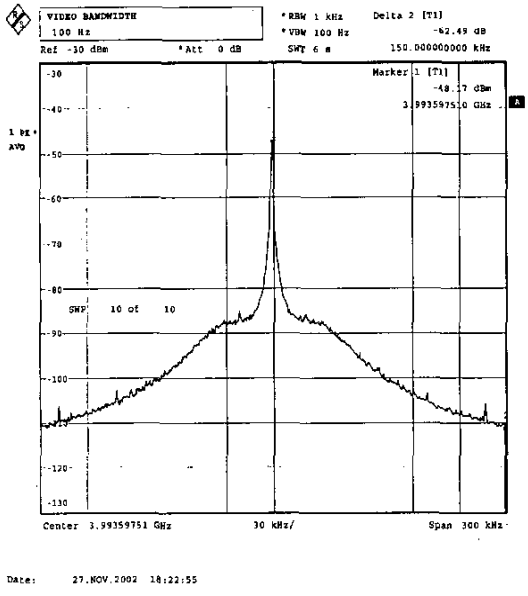

Figure 7. Carrier out-power spectral density, span: 300kHz.

The VCO phasenoise within the loop band width of 30kHz is clearly suppressed. The carrier frequency can be switched from 3.8GHz to 4.05GHz in 400kHz steps. The VCO dissipates 4.1mW from a 2.2V supply, all other blocks are biased at 1.5V. The total power consumption of the synthesizer can be stated with 10.2mW.

V. CONCLUSIONS

The design of a 4GHz phase-locked loop with dual-mode tuning technique has been presented. The synthesizer was fabricated using a 0.12µm standard CMOS-process. The technical realization of the fully-integrated VCO to support dual-mode tuning has been explained. Phase-noise and tuning measurements of the free-running VCO were shown. The proposed dual-mode tuning technique works properly over the specified tuning range. The benefits due to dual-mode tuning were discussed in detail. The complete system dissipates only 10.2mW.

VI. ACKNOWLEDGMENTS

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REFERENCES

[1] C. P. Yue, C. Ryu, J. Lau, T. H. Lee, S. S. Wong, "A Physical Model for Planar Spiral Inductors on Silicon" in 1996 Int. Electron Dev. Meeting Dig. Tech. Pappers, pp. 155-158, Dec. 1996

[2] J. Craninckx, M. S. J. Steyaert, "A 1.8GHz Low-Phase-Noise CMOS VCO Using Optimized Hollow Spiral Inductors", IEEE Journal of Solid-State Circuits, vol. 32, no. 5, pp. 736-744, May 1997

[3] A. Hajimiri, T. H. Lee, "The Design of Low Noise Oscillators", Kluwer 1999

[4] Thomas H. Lee "The Design of CMOS RF Integrated Circuits" , Cambridge University Press, 1998

[5] N. Da Dalt, S. Derksen, P. Greco, C. Sandner, H. Schmid, K. Strohmayer, "A Fully Integrated 2.4GHz LC-VCO Frequency Synthesizer with 3ps Jitter in 0.18µm Standard Digital CMOS Copper Technology", Proceedings of the 27th European Solid-State Circuits conference, pp. 508-511, Sept. 2001

[6] B. Razavi "Monolithic Phase-Locked Loops and Clock Recovery Circuits: Theory and Design", ISBN 0-7803-1149-3, 1996

[7] M. Tiebout "A 480µW, 2GHz ultra low power dual modulus prescaler in 0.25µm standart CMOS" Proceedings of ISCAS 2000, vol. 5, pp. 741-744, May 2000

[8] G. Konstanznig, T. Pappenreiter, L. Maurer, A. Springer, R. Weigel „Design of a 1.5V, 1.1mA Fully Integrated LC-tuned Voltage Controlled Oscillator in the 4GHz-Band using a 0.12µm CMOS-process" 2002 Asia-Pacific Microwave Conference Proceedings, pp. 1471-1474, Nov. 2002

[9] P. Andreani and S. Mattison, "On the Use of MOS varactors in RF VCO's" *IEEE J. Of Solid-State Circuits*, Vol. 35, No.6, pp. 736-744, June 2000